What is claimed is:

1. A semiconductor package comprising:

an interim substrate having a front surface and a back surface;

a solder mask formed at selected locations on the front surface of the interim substrate;

a lead layer and a die pad layer formed on the front surface of the interim substrate not covered by the solder mask;

a chip adhering to the die pad layer;

a plurality of conductive elements electrically connecting the chip and lead layer; and

a molded resin covering the chip, conductive elements, solder mask, lead layer and die pad layer;

wherein the interim substrate is etched after the semiconductor package is singulated for obtaining the semiconductor package without substrate.

2. The semiconductor package of claim 1, wherein the interim substrate is made of copper.

3. The semiconductor package of claim 1, wherein the solder mask is made from photosensitive and insulative materials selected from the group consisting of polyimide or ultraviolet-curable resin.

4. The semiconductor package of claim 1, wherein the lead layer and die pad layer are made of conductive materials consisting of nickel and gold.

5. The semiconductor package of claim 1, wherein the solder

mask is formed by performing photolithography process on a polyimide or ultraviolet-curable resin layer formed at selected locations of the front surface of the interim substrate.

6. The semiconductor package of claim 1, wherein the lead layer and die pad layer are formed by plating.

7. The semiconductor package of claim 1, wherein the conductive elements are made of a material selected from the group consisting of gold, copper or aluminum.

8. The semiconductor package of claim 1, wherein the die pad layer is replaced by a solder mask.

9. A method of manufacturing a semiconductor package comprising the following steps:

a. setting up an interim substrate which has a front surface and a back surface;

b. forming a solder mask which covers selected locations of the front surface of the interim substrate;

c. forming a lead layer and a die pad layer on the front surface of the interim substrate not covered by the solder mask;

d. adhering the bottom side of a chip to the top side of the die pad layer;

e. connecting electrically the chip and the lead layer by a plurality of conductive elements;

f. encapsulating the solder mask, chip, die pad layer, lead layer and conductive elements with a molded resin;

g. singulating the semiconductor package; and

h. removing the interim substrate by etching process for forming the semiconductor package without substrate.

10. The method according to claim 9, wherein the interim substrate is made of copper.

11. The method according to claim 9, wherein the solder mask is made from photosensitive and insulation materials selected from the group consisting of polyimide or ultraviolet-curable resin.

12. The method according to claim 9, wherein the lead layer and die pad layer are made of conductive materials consisting of nickel and gold.

13. The method according to claim 9, wherein the solder mask is formed by performing photolithography process on a polyimide or ultraviolet-curable resin layer formed at selected locations on the front surface of the interim substrate.

14. The method according to claim 9, wherein the lead layer and die pad layer are formed by plating.

15. The method according to claim 9, wherein the conductive elements are made of a material selected from the group consisting of gold, copper or aluminum.

16. The method according to claim 9, wherein the die pad layer is replaced by a solder mask.